Connecting AMD Flash Memory to a System Address Bus

AMD

Application Note

This document is intended to clarify how Flash memories may be connected to a system address bus and how software should issue device commands to Flash devices.

Organization Modes

All AMD Flash devices have either a byte-wide internal organization or can be used in "byte mode," a mode that presents a byte-wide organization to the system. Some AMD Flash devices can also present a 16-bit-wide organization to the system. This is referred to as "word mode."

Nomenclature

Most single-power-supply AMD Flash devices have part numbers that begin with "Am29," followed by one or two letters that indicate the technology used in the particular family of devices. An "F" indicates 5 V devices. The letters "LV" indicate "low voltage," and refer to devices that may operate as low as 2.7 V. The letters "DL" indicate dual-bank (read-while-write) and low voltage. Following the letters are three digits that indicate the density and organization of the Flash device. In general, Flash memories that only provide a byte wide (x8-only) organization have numbers less than 100. The Flash memories that support both byte and word modes have numbers greater than or equal to 100. See Table 1 for examples.

Dual organization (x8/x16) modes allow for use in a wider range of systems, which may be either byte or word addressed.

Table 1. AMD Flash Nomenclature

Am29	F (5 V)	040 (4 Mbit, x8-only)
	LV (2.7 V)	002 (2 Mbit, x8-only)
		400 (4 Mbit, x8/x16)
	DL (2.7 V dual bank)	162 (16 Mbit, x8/x16)
		322 (32 Mbit, x8/x16)
	SL (1.8 V)	800 (8 Mbit, x8/x16)

Flash Address Pin Labels

The address pins for byte-wide-only Flash devices are labeled A0 to AN, where N is the highest order address bit. A0 is the address bit that selects the odd or even byte.

The address pins for dual organization memories are labeled in terms of word selection. In word mode, all data lines (DQ0 through DQ15) are used to convey a data word. The address bus of the flash device is used to select data on word boundaries and the pins are labeled as A0 through AN, where N is the highest order address bit. A0 is the address bit that selects the odd or even word. Each unique address placed on the address bus selects an individual word to be read or programmed. In word mode there is no means to individually select a byte within a word.

In byte mode, the upper data lines are not needed for data. Seven of these data lines (DQ8–DQ14) are placed into a tri-state mode, and DQ15, the highest order *data* bit, functions as the lowest order *address* bit, and is referred to as A-1 (read "A minus 1," to indicate that the bit is one order lower than A0). Byte data is placed on DQ0 through DQ7, and is addressed by bits A-1 through AN, where N is the highest order address bit on the Flash device. In byte mode each unique address placed on the address bus selects an individual byte to be either read or programmed.

Word Mode Address Interface

A common situation is a byte-addressed processor, which is connected to a flash device used in word mode (Shown in Figure 1). In this configuration, the System (processor) Address word selector bit (labeled SA1) is connected to the Flash A0 bit. Since the processor byte selector bit SA0 is not connected, the Flash may only be addressed on word boundaries and appears as contiguous word storage locations.

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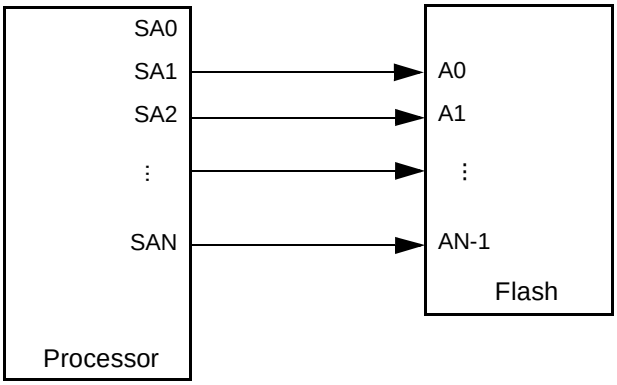

Figure 1. Byte Address Processor Connected to Word Mode Flash

Another common situation is a byte-addressed processor connected to either a x8 Flash device (Figure 2), or a x8/x16 Flash device operated in byte mode (Figure 3). In this case each consecutive byte access from the processor needs to select a specific byte in the Flash memory array. The System Address byte selector (SA0) is connected to the Flash LSB address (which is labeled A0 in x8-only devices, and DQ15/A-1 in x8/x16 devices).

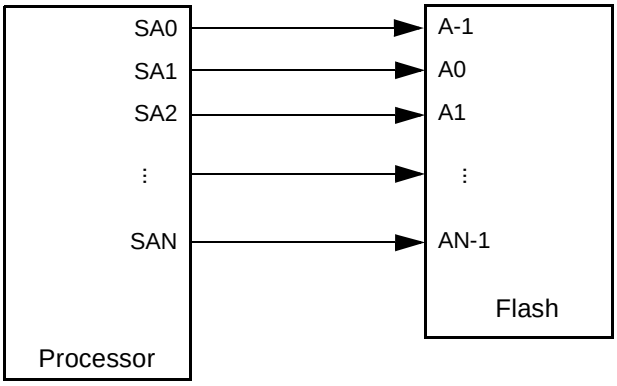

Figure 2. Byte Address Processor Connected to Byte Mode x8/x16 Flash

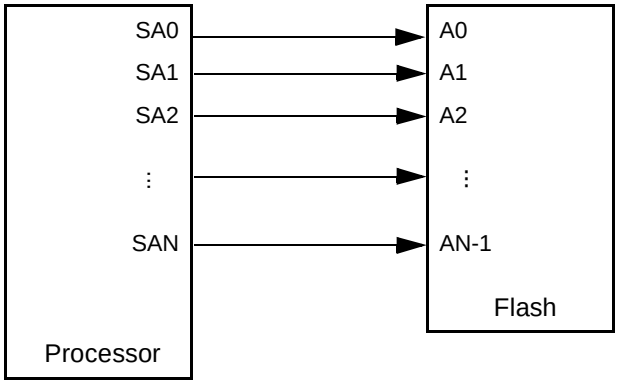

Figure 3. Byte Address Processor Connected to x8-only Flash

Note: *The DQ15/A-1 bit only appears in x8/x16 devices. When operating in x8 mode, the A-1 bit is the LSB bit of the Flash. In x16 (or word) mode, A0 becomes the LSB. In x8-only devices, the A0 bit is the LSB for the Flash.*

AMD Flash devices can also be used in parallel, such as might be the case when using two x8-only devices in parallel on a 16-bit data bus (Figure 4). This situation is extensible to 32-bit processor buses when combined with four byte-wide devices in parallel (Figure 5), or two word-wide devices in parallel (Figure 6). In these cases the memories are being treated as portions of a wider memory and the system address lines connected to the memories must reflect this by having higher order system address lines connected to lower order Flash address inputs.

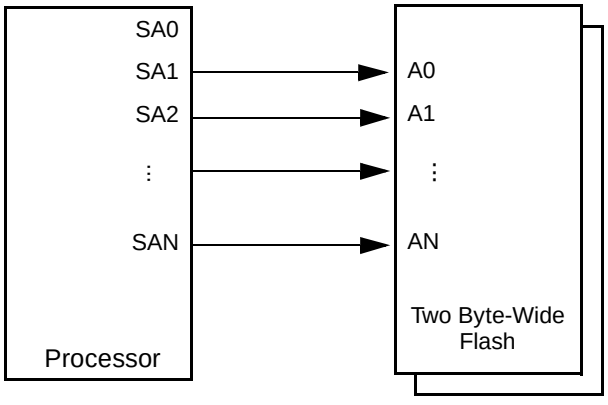

Figure 4. Byte Address Processor Connected to Two x8-only Flash on a 16-Bit-Wide Data Bus

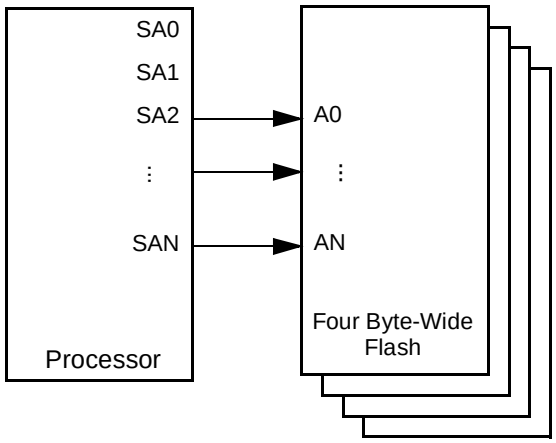

Figure 5. Byte Address Processor Connected to Four x8-Only Flash on a 32-Bit-Wide Data Bus

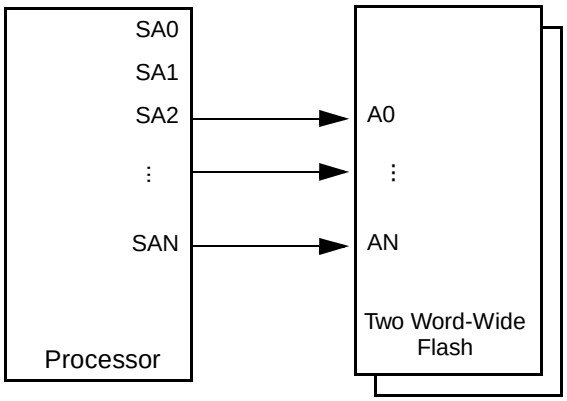

Figure 6. Byte Address Processor Connected to Two x16 Flash on a 32-Bit-Wide Data Bus

Constructing Address Tables

What is important from the above system examples is to note that the mapping between processor address lines and Flash address lines changes depending on the Flash device mode in use and number of Flash devices used in parallel. When commands are written to Flash, the device expects certain address value patterns. System designers must therefore supply the expected address patterns and values from the viewpoint of the Flash device.

To help visualize the pin mapping and processor address value adjustments, a table similar to Table 1 might be constructed.

Table 2. Address Line Relationships

Description	Address Lines & Values (Note 1)											
System Address	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
x8-only Flash (Note 2)	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
x8/x16 Flash Byte Mode (Note 2)	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A-1
x8/x16 Flash Word Mode (Note 3)	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
System Binary Address	1	0	1	0	1	0	1	0	1	0	1	0
Flash Hex Address (x8/x16 device in word mode)	5			5				5				
Flash Hex Address (x8-only device or x8/x16 device in byte mode)	A				A				A			

Notes:

1. *Table assumes processor provides a byte-selecting system address.*
2. *Assumes single Flash memories are used to provide a byte-wide data bus.*
3. *Assumes single Flash memories are used to provide a word-wide data bus.*

A repeating pattern of hex “A” characters on the system address bus would appear as a pattern of hex “A” characters to a byte-wide-only flash connected to the processor because the system and Flash address lines are connected with matching address line significance—the A0 of the Flash is tied to the SA0 of the processor (refer to Table 2, bottom row). However, the same pattern of hex “A” characters presented to a x8/x16 Flash used in the word mode would appear to that device as if it were a repeating pattern of hex “5” char-

acters (refer to Table 2, second row from bottom). When used in word mode, the device's least significant address A0 is connected to the SA1 address line. This is why a Flash device command table shows a different address pattern for x8/x16 Flash devices depending on whether byte or word mode is in use. These command tables are always defined from the viewpoint of the Flash device's address bus.

Table 3 lists the Flash Command Definitions table for the Am29LV800B Flash Device.

Table 3. Am29LV800B Command Definitions

Command Sequence			Cycles	Bus Cycles											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22DA				
		Byte		AAA		555		AAA		X02	DA				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	225B				
		Byte		AAA		555		AAA		X02	5B				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program			2	XXX	A0	PA	PD								
Unlock Bypass Reset			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	XXX	B0										
Erase Resume			1	XXX	30										

For each command listed in Table 3, there is an associated set of address/data patterns that must be written in a particular sequence in order to instruct the Flash device to perform specific functions. It can also be seen that the address requirements for each command appear different depending on the Flash operating mode.

The command definition tables provided in all AMD Flash data sheets are structured in a way to represent what the Flash is required to "see" on its address pins for a particular operation to execute. Since the Flash may be connected in different ways (as illustrated earlier), the values in the address tables may need to be "shifted" when writing Flash software driver code, to reflect the processor and Flash address bus relationship, in order for the Flash device to recognize the proper bit patterns.

Notice that in Table 3 the first command address pattern for a x8/x16 Flash, operating in byte mode, should be a set of repeating hex "A" characters. From the viewpoint of the Flash, its address lines are connected to the processor address lines of the same significance. The Flash address lines are labeled A-1 through AN.

Alternatively, if a x8/x16 Flash is used in word mode, there is no A-1 address pin and its lowest significance address line A0 is connected to the SA1 processor address line. From the word mode Flash viewpoint the pattern is a set of repeating hex "5" characters, as shown in Table 3. However, from the processor's viewpoint it is the same pattern shown in Table 2. It is still a byte address of "AAA" hex as far as the processor (and the software developer writing the Flash driver code) is concerned. This is often a point of confusion for authors of Flash driver code. Developers therefore should

be aware that the tables in AMD Flash data sheets are from the Flash viewpoint, but that the code has to be constructed from the processor viewpoint.

The most common system implementations use a x8/x16 Flash in either byte mode as a single byte-wide memory, or in word mode as a single word-wide memory. *When writing software drivers for either of these cases, use the patterns shown for the byte mode*. Since the address connections between the processor and the Flash are already offset properly, the Flash device will accept those addresses.

For these common system configurations, software drivers have already been written for AMD Flash memories. These are available as C source code via the AMD web-site (www.amd.com) or the local AMD sales office.

When Flash devices are used in parallel to serve a wider data bus the relative positions of processor and Flash address lines will shift more as shown in Figures 4, 5, and 6. So, the expected patterns shown in the command table must be shifted up in the processor code viewpoint so that the patterns remain on the desired pins of the Flash address bus (an exercise left for the reader).

Some Address Lines Don't Care

Not all address lines are checked for the hex address patterns by the Flash memory. These upper address lines are "don't care" from the viewpoint of any particular Flash device. However, exactly which lines are ignored varies with different Flash devices. Always check the notes below the bus command table in the datasheet to know which address lines do not require the hex pattern. However, placing the pattern on all the address pins has no effect on address bits that are "don't care."

Handling Bank, Sector, and Programming Offsets

In certain commands, a bank, sector, or programming offset address must be given in order for the command to correctly begin. Flash address bits above A10 are used for these purposes.

Bank addresses (listed as "BA" in AMD data sheets) are used in the AMD DL (Simultaneous Read-Write) devices to uniquely identify one of two specific banks. For example, the Am29DL800B data sheet specifies that address bits A16 through A18 uniquely select a specific bank. For larger density devices, Flash address bits A16 through the MSB of the Flash device uniquely identify a bank.

Sector Addresses (SA in AMD data sheets) are used for sector specific Flash operations (such as Sector Erase and Sector Protect Verify). Address bits from A12 to the MSB are used to uniquely specify a sector.

The Program Address Offset (PA in AMD data sheets) is simply an offset from the beginning of the device into the Flash Array. Since this offset is not bank or sector specific, it is simply the desired byte offset into the array in which data will be programmed. Since this offset address can span more that 10 bits (past Flash address bit A10), those address bits higher than A10 are no longer considered "don't cares."

Flash sector and bank sizes are always quoted in terms of bytes in the datasheets. In the most common system implementation using a single byte or word mode Flash, the system byte address of the processor matches with the quoted sector address boundaries since both are in terms of bytes. There is no special adjustment needed for the system address in these common system implementations. However, where parallel Flash devices are used on a wider data bus, the bank, sector, and programming offset addresses will have to be shifted up to match the Flash device viewpoint.

Conclusion

The Flash memory command definition tables found in all AMD Flash datasheets always show addresses from the viewpoint of the Flash address pins in use for the particular mode (byte or word). These tables also assume a system where the Flash memory is in an organization mode that matches the width of the data bus. Those who write software drivers for Flash devices must consider the system implementation of single versus parallel Flash devices when determining the degree to which addresses shown in the command tables may need to be shifted up in order for Flash devices to properly recognize the Flash commands.

For the most common system configurations, software drivers have already been written for AMD Flash memories. These are available as C source code via the AMD web-site (www.amd.com) or the local AMD sales office.